

## ST20P64 模擬 ST2032 注意事項

### 1. ST20P64 比 ST2032 多出下列 Control Register :

#### 1.1 Port-A used as keyboard return line selection

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
\$00E	PAK	R/W	PAK[7]	PAK[6]	PAK[5]	PAK[4]	PAK[3]	PAK[2]	PAK[1]	PAK[0]	0000 0000

Bit 7~0: **PAK[7~0]** :  
 1 = Port-A used as keyboard return line.  
 0 = Port-A used as keyboard normal I/O.

用來模擬 ST2032 時請保持 Default 。

#### 1.2 COMMON Output Register

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
\$036	COM	R/W	COM[7]	COM[6]	COM[5]	COM[4]	COM[3]	COM[2]	COM[1]	COM[0]	???? ????

用來模擬 ST2032 時當做沒有此 byte 。

#### 1.3 Control Register For PSG Output

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
\$015	PSGC2	R/W	-	-	-	-	PSGOD	PSGOBD	PSGOE	PSGOBE	---- 1111

Bit 3: **PSGOD** : Data bit if PSGO is used as normal output pin.  
 1 = PSGO is output High.  
 0 = PSGO is output Low

Bit 2: **PSGOBD** : Data bit if PSGOB is used as normal output pin.  
 1 = PSGOB is output High.  
 0 = PSGOB is output Low

Bit 1: **PSGOE** : PSG output enable bit  
 1 = PSGO is PSG data output pin.  
 0 = PSGO is normal output pin

Bit 0: **PSGOBE** : PSG inverse signal output enable bit  
 1 = PSGOB is PSG inverse data output pin.  
 0 = PSGOB is normal output pin

用來模擬 ST2032 時請保持 Default 。

#### 1.4 ROM Bank Selection Registers (\$32)

Address	Register	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DRR	\$32	RW	-	-	-	-	-	-	-	DRR0

用來模擬 ST2032 時請保持 Default 。

2. ST20P64 在原有的 Register 比 ST2032 多出下列 Control Bit :

2.1 Port Function Control Register

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
\$00F	PMCR	R/W	PULL	PDBN	INTEG	-	PAPR	-	-	-	100 - 0 - - -
Bit3: <b>PAPR</b> : Pull-up resistor option bit 1 = Large pull-up resistor 0 = Normal pull-up resistor											

用來模擬 ST2032 時請保持 Default。

2.2 LCD Segment Number Selection Register

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
\$039	LSEL	R/W	DUTY[1]	DUTY[0]	BIAS4	LSEL[4]	LSEL[3]	LSEL[2]	LSEL[1]	LSEL[0]	0001 1111
Bit 7~6: <b>DUTY[1:0]</b> : LCD duty selection 0X = 1/16 duty 10 = 1/12 duty 11 = 1/8 duty  Bit 5: <b>BIAS4</b> : LCD bias selection 1 = 1/4 bias 0 = 1/5 bias											

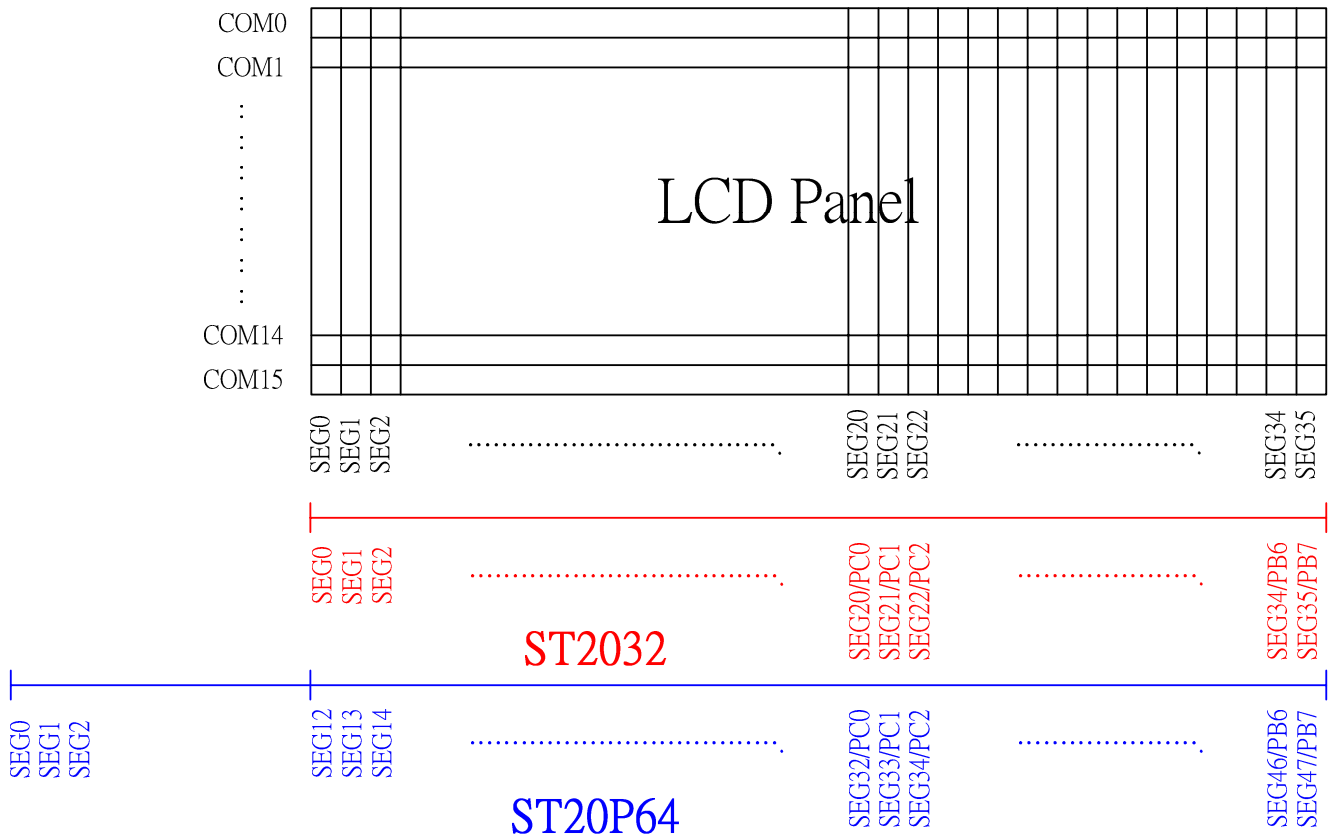
在 ST20P64 中，在 LCD ON 時更動 DUTY 或 BIAS 會使 LCD 發生錯誤，欲改變 DUTY 或 BIAS 時請先將 LCD OFF。用來模擬 ST2032 時請保持 Default。

2.3 LCD Clock Source and Driving Strength Control Register

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
\$03B	LCK	R/W	DRV[3]	DRV[2]	DRV[1]	DRV[0]	PUMPB	LCK[2]	LCK[1]	LCK[0]	1111 -000
Bit 3: <b>PUMPB</b> : 1 = Without DC-DC voltage converter for LCD driver 0 = With DC-DC voltage converter for LCD driver											

在 ST20P64 中”PUMPB”及 LCD Frame Rate Control “LCK”只有在 LCD OFF 時才能寫入，在做 Frame Rate 調整時請注意 LCD 的狀態。

### 3. ST20P64 的 LCD Segment 需調整：



因為 ST20P64 的 Segment 數比 ST2032 多出 12 個，所以 ST20P64 的 SEG12~SEG47 與所 Share 的 I/O 順序的排列，才會與 ST2032 的 SEG0~SEG35 相同。除了在貼玻璃時要注意外，在程序上 LCD RAM 的範圍也要再做 Shift(\$1000+12~\$1023+12, \$1080+12~10A3+12)。

- ST20P64 有一個對 LCD Segment nonselection(V2,V3)的穩壓電容，在模擬 ST2032 時要將此電容拔除，會較接近真實的 ST2032 的 Display Quality。
- R-oscillator 在同一個頻率下(3V)，ST20P64 的阻值會比 ST2032 來得大。

Vcc=3V	ST20P64	ST2032
2MHz	260KΩ	110KΩ
4MHz	110KΩ	47KΩ